MODELING OF NOISE PARAMETERS OF MESFET'S AND MODFET'S AND THEIR FREQUENCY AND TEMPERATURE DEPENDENCE

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ABSTRACT

A simple wideband noise model of microwave MESFET (MODFET, HEMT, etc.) is described and verified at room and cryogenic temperatures. Closed form expressions for T_{min} - minimum noise temperature, Z_{gopt} - optimum generator impedance, g_n - noise conductance are given in terms of frequency, the elements of FET equivalent circuits, and the equivalent temperatures of intrinsic gate resistance and drain conductance. The model allows prediction of the noise parameters for a broad frequency range from a single frequency measurement of noise parameters.

INTRODUCTION

The modeling of noise performance of field-effect transistors (FET's) has been a subject of study for more than a quarter of a century (for instance [1]-[5]). A novelty of the approach presented in this paper rests in the demonstration that for an intrinsic device two frequency independent constants (equivalent temperatures of intrinsic gate resistance and drain conductance), need to be known, in addition to the elements of an equivalent circuit, to predict all four noise parameters at any frequency. Surprisingly, it is also shown that at both room and cryogenic temperatures the effective gate temperature is within measurement errors equal to the ambient temperature of the device.

NOISE PARAMETERS OF A FET CHIP

An equivalent circuit of a FET chip is shown in Figure 1. Parasitic resistances contribute only thermal noise and with the knowledge of the ambient temperature T_a their influence can be easily taken into account [7], [8]. The noise properties of an intrinsic chip are then treated by assigning equivalent temperature T_g and T_d to the remaining resistive (frequency independent) elements of the equivalent circuit r_{gs} and g_{ds}, respectively.

The noise parameters of an intrinsic chip of Figure 1 can be found to be:

$$T_{min} = 2\frac{f}{f_t}\sqrt{g_{ds}\, r_{gs}\, T_g\, T_d + \left(\frac{f}{f_t}\right)^2 r_{gs}^2\, g_{ds}^2\, T_d^2} + 2\left(\frac{f}{f_t}\right)^2 r_{gs}\, g_{ds}\, T_d \qquad (1)$$

$$R_{opt} = \sqrt{\left(\frac{f_t}{f}\right)^2 \frac{r_{gs}}{g_{ds}}\frac{T_g}{T_d} + r_{gs}^2} \qquad (2)$$

$$X_{opt} = \frac{1}{\omega\, C_{gs}} \qquad (3) \qquad g_n = \left(\frac{f}{f_t}\right)^2 \frac{g_{ds}\, T_d}{T_o} \qquad (4)$$

where $f_t = g_m/(2\pi\, C_{gs})$. Also

$$\frac{4NT_o}{T_{min}} = \frac{2}{1 + \frac{r_{gs}}{R_{opt}}} \qquad (5)$$

where $N = R_{opt}\, g_n$.

If the noise parameters of a MESFET (MODFET) can be described by the model, then the measured ratio of $4NT_o/T_{min}$ must satisfy

$$1 \le \frac{4NT_o}{T_{min}} < 2 \qquad (6)$$

at all frequencies. The left hand side inequality is quite fundamental [9], [10] while the right hand side is a limitation of the model only. Inequality (6) can provide a fast check of the validity of the model and also an insight into the nature of noise sources within the transistor, without any knowledge of the transistor equivalent circuit or intervening lossless two-port. The inclusion of other elements of the equivalent circuit of a chip can be done quite generally in a computer routine using the relations published in [7] and [8].

EXPERIMENTAL VERIFICATION

The model described in the previous section by a proper choice of constants T_g, T_d may represent the noise processes in the intrinsic chip which at

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the gate-source and drain-source terminals produce partially correlated noise currents with a purely imaginary correlation coefficient. The noise constants T_g and T_d need to be determined from a measurement but if the equivalent circuit of a chip and its noise parameters at some frequency are known, the determination is straightforward.

An equivalent circuit of a FHR01FH HEMT is shown in Figure 2. The values of the elements of the equivalent circuit were found from Fujitsu S-parameter data for both chip and packaged devices at bias V_{ds} = 2V, I_{ds} = 10 mA [11]. The comparisons between the S-parameters predicted from the model and those measured by Fujitsu for the packaged (FHR01FH) device are shown in Figure 3. The noise parameters of the FHR01FH device (lot #C923) for the room and cryogenic temperatures were given at frequency f = 8.5 GHz in a previous paper [6]. The equivalent temperatures T_g and T_d were determined by finding first the noise parameters of an intrinsic chip and then using equations (1)-(4) to provide the best fit in mean square sense to the deembedded noise parameters. This process is summarized in Tables I and II.

The knowledge of the equivalent temperatures T_d, T_g and the elements of the equivalent circuit at a given ambient temperature T_a allows computation of noise parameters at any frequency. The computed results for the FHR01FH device (packaged) and the FHR01X device (chip) at 297 K and 12.5 K are shown in Figures 4, 5, and 6. They are also compared with available experimental results. The agreement of measured and model predicted results over the 4 to 22 GHz range should be judged excellent.

DISCUSSION AND CONCLUSIONS

Among many observations that can be made about the theory of section II and the experimental results of section III, two are the most important. First, the expressions of Pucel *et al.* [2] for the noise parameters of an intrinsic chip under small frequency approximation can be found identical to (1)-(4) if:

$$K_g = \frac{g_{ds}}{g_m}\,\frac{T_d}{T_o}\,, \quad K_r = g_m\, r_{gs}\,\frac{T_g}{T_o}\,, \quad K_c = 1 \qquad (7)$$

where K_g, K_r and K_c are dimensionless noise coefficients defined in [2]. Second, an assignment of an equivalent gate temperature to the intrinsic gate resistance models a noise process within a FET which produces perfectly correlated short-circuit noise currents in the drain and gate with a purely imaginary correlation coefficient, while an assignment of T_d to the drain conductance models a noise process which produces noise current only in a drain circuit. If, as postulated in [2], the gate noise current of an intrinsic chip was indeed induced by the drain current fluctuations, then the rate of decrease of T_d and T_g upon cooling should be about the same. The data of Table II do not confirm this observation, showing T_g to be in both cases close to the ambient temperature of the device.

In conclusion, the noise parameters of a FET were found to be functions of the elements of a small signal equivalent circuit of a FET and two frequency independent constants, named equivalent gate and drain temperatures. The equivalent temperatures in the example of a FHR01FH MODFET were demonstrated to be independent of frequency in the frequency range in which 1/f noise is negligible. Thus, the model allows prediction of noise parameters for a broad frequency range from a single frequency noise parameter measurement.

The model uses only circuit theory concepts and, therefore, it is very easy to implement in any CAD and/or CAM package. Finally, it is hoped that it may be used by device manufacturers as a standard noise description of commercial devices.

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TABLE I. Noise Parameters of FHR01FH at Different Stages of Deembedding

f = 8.5 GHz, V_{ds} = 2 V

	T_a = 297 K, I_{ds} = 10 mA				T_a = 12.5 K, I_{ds} = 5 mA			
NOISE PARAMETERS	T_{min} K	R_{opt} Ω	X_{opt} Ω	g_n mS	T_{min} K	R_{opt} Ω	X_{opt} Ω	g_n mS
PACKAGED FET	78.0	10.5	17.5	9.4	10.0	4.4	17.0	2.6
FET CHIP	79.1	26.3	53.8	3.8	10.1	11.2	57.2	1.0
INTRINSIC CHIP WITH C_{gd}	64.6	20.7	53.7	3.8	8.1	8.8	57.2	1.0
INTRINSIC CHIP WITHOUT C_{gd}	65.6	26.3	59.5	3.0	8.2	11.4	65.2	.80

TABLE II. Comparisons of Noise Parameters of FHR01 Intrinsic Chip

f = 8.5 GHz

T_a K	Comments	T_{min} K	R_{opt} Ω	X_{opt} Ω	g_n mS	T_g K	T_d K
297	From Table I	65.6	26.3	59.5	3.0	-	-
	Model Best Fit	58.7	28.4	66.9	3.27	304	5514
12.5	From Table I	8.2	11.4	65.2	.80	-	-
	Model Best Fit	7.4	12.3	66.9	.87	14.5	1406

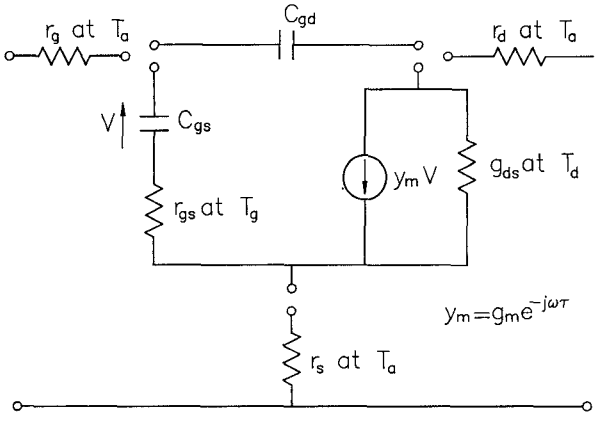

FIG. 1: Equivalent circuit of a FET (HEMT, MODFET) chip. Noise properties of an intrinsic chip are represented by equivalent temperatures: T_g of r_{gs}, and T_d of g_{ds}. Noise contribution of ohmic resistances r_s, r_g and r_d are determined by physical temperature T_a of a chip.

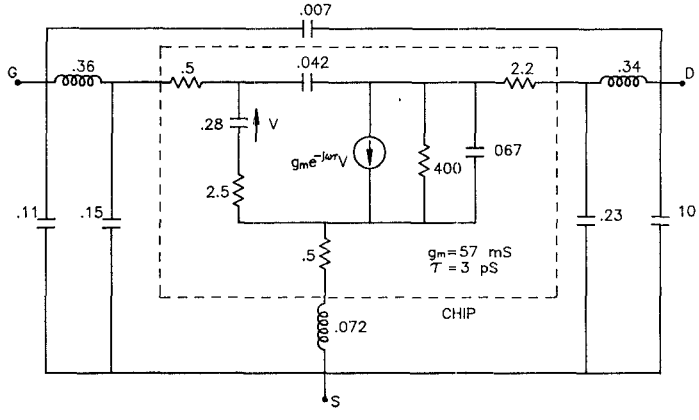

FIG. 2: Equivalent circuit of FHR01FH HEMT at T_a = 297 K, V_{ds} = 2 V, I_{ds} = 10 mA. Values of resistance, capacitance and inductance are given in ohms, picofarads and nanohenries.

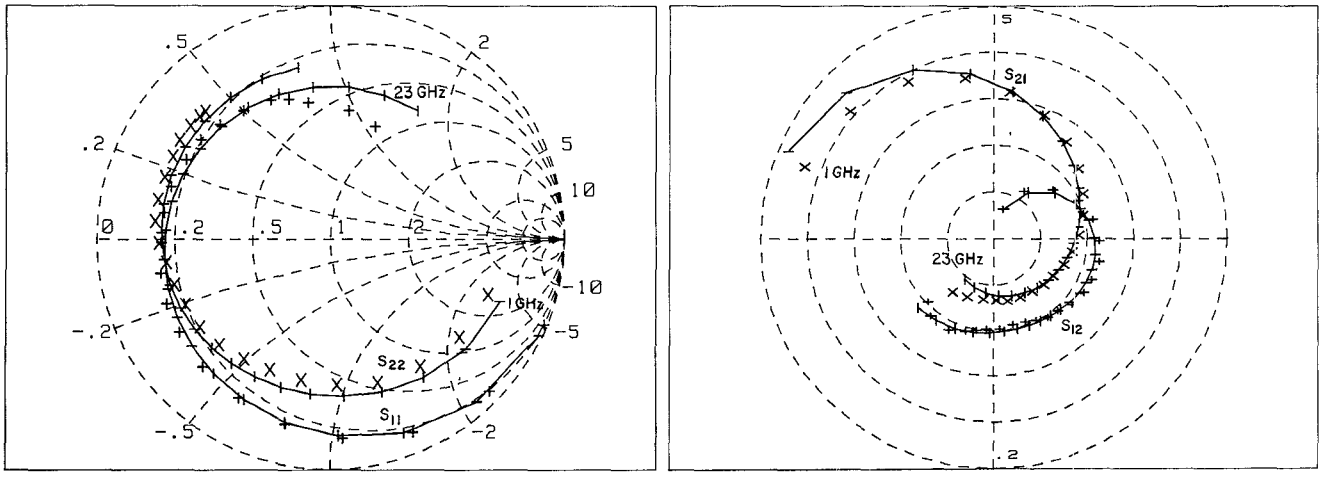

FIG. 3: Comparison between S-parameters of FHR01FH measured by Fujitsu [11] and those predicted from model of Figure 2. Lines with ticks are for computed data while crosses indicate measured points.

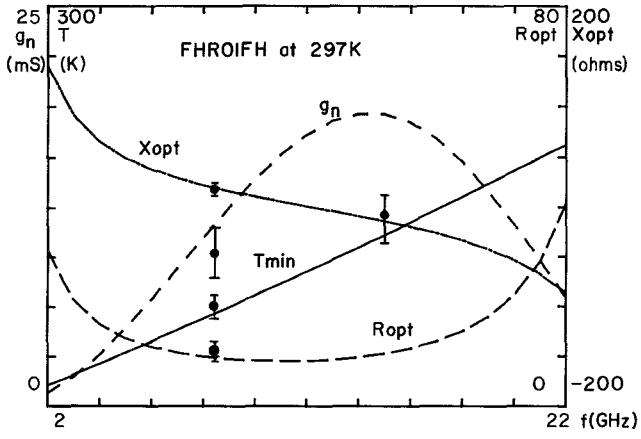

FIG. 4: Noise parameters and associated gain of FHR01FH HEMT at T_a = 297 K and V_{ds} = 2 V, I_{ds} = 10 mA. Lines indicate data obtained from the model using the equivalent circuit of Figure 2, T_g = 304 K and T_d = 5514 K. Points indicate data from [6] and [12].

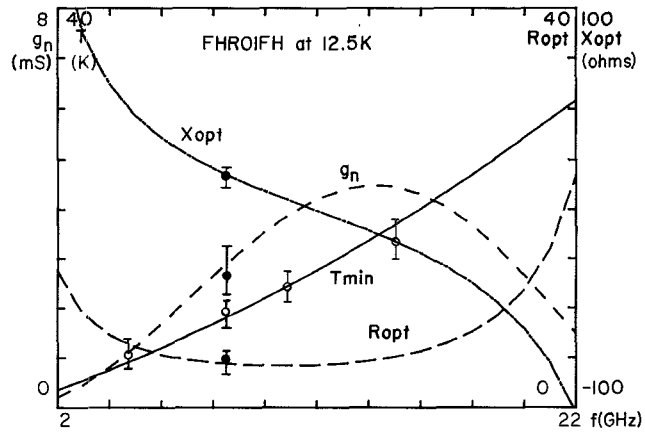

FIG. 5: Noise parameters and associated gain of FHR01FH HEMT at T_a = 12.5 K and V_{ds} = 2 V, I_{ds} = 5 mA. Lines indicate data obtained from the model using equivalent circuit of Figure 2, g_m = 50 mS, r_{ds} = 500 Ω, T_g = 14.5 K and T_d = 1406 K. Points indicate experimental data from [6] and [12].

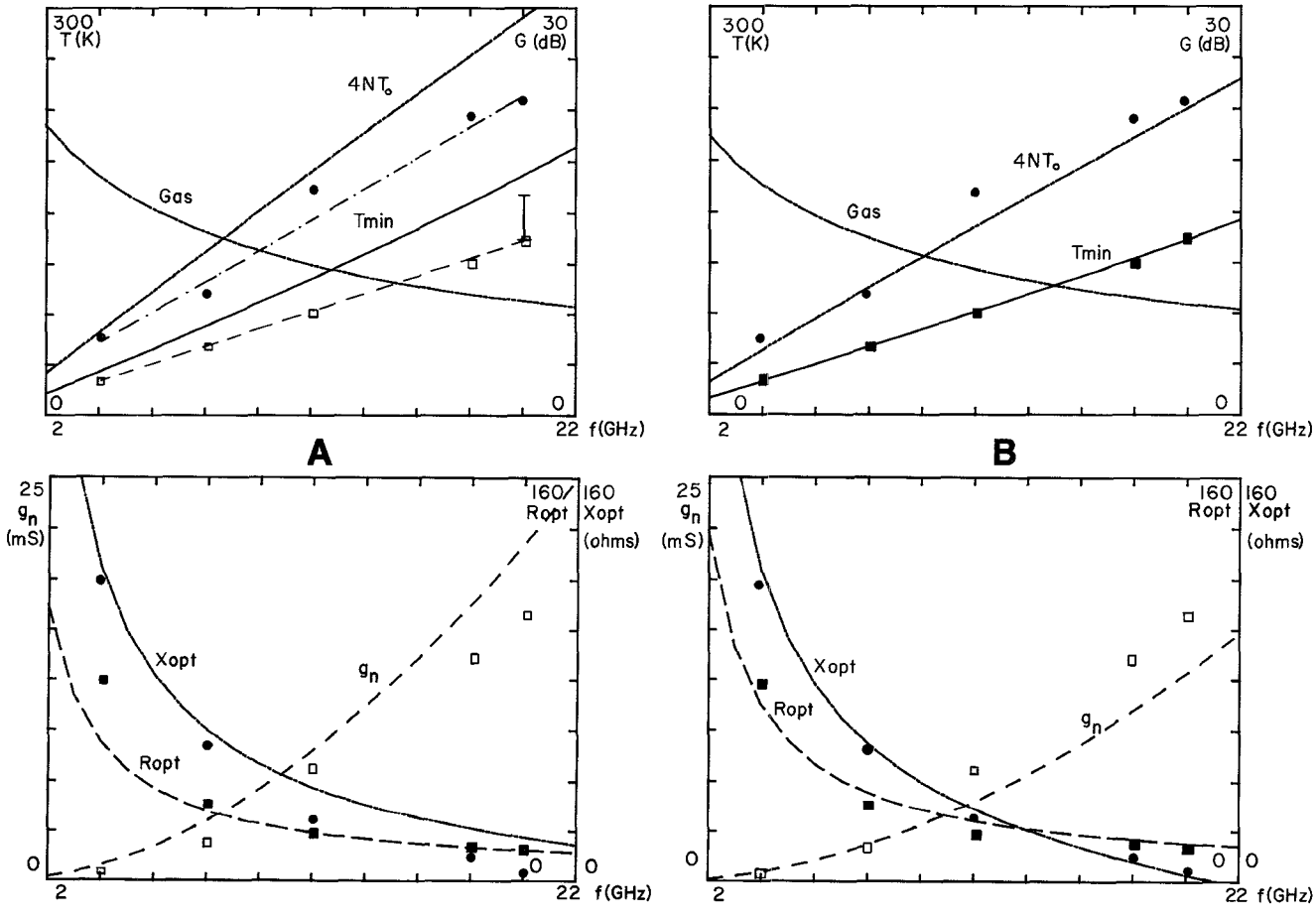

FIG. 6: Comparison of noise parameters of FHR01X (chip) HEMT at room temperature computed from the model with experimental results from Fujitsu data sheet [11]. For computations, a part of the equivalent circuit of Figure 2, denoted by broken lines with source inductance added, was used.

(A) For the model data T_g = 304 K, T_d = 5514 K, T_a = 297 K were used. T_g and T_d were determined from a single noise parameter measurement of a package device (lot #C923) at 8.5 GHz.

(B) For the model data $T_g = T_a$ = 297 K was assumed and T_d = 3364 K was found to fit best Fujitsu measured data. Also, the equivalent circuit of a chip was amended with parasitic gate inductance L_g = .12 nH.